ADVISORS

Rev. Sr. B. Hamlet, M.E.,
Administrator.

Dr. M. Rajkumar, M.E., Ph.D.,
Principal.

CONVENOR

Mrs.M.Shenbagavalli, M.Tech.,(Ph.D.),
Head / ECE, JPCOE.

CO-ORDINATORS

Dr. S. D. Jayavathi, M.E., Ph.D.,
Professor / ECE.

Dr. E. A Mohamed Ali, M.E., Ph.D.,
Associate Professor / ECE.

COMMITTEE MEMBERS

Dr.P.Nelson Kingsley Joel, AP/ECE.
Mr.G.Vinoth Rajkumar, AP/ECE
Ms.M.Stella Rose Malar, AP/ECE
Mr.M.Paramaiyappan, AP/ECE.
Mrs.M.Vijaya Gandhi, AP/ECE.
Mr.V.Ayyappan, AP/ECE.
Mrs.R.Chandrika, AP/ECE.
Mrs.B.Priyanka, AP/ECE
Ms.R.Rajeshwari, AP/EEE

ABOUT THE COLLEGE

J.P. College of Engineering (JPCOE) was started in the year 2008. JPCOE is a self-financing, co- educational Engineering College and it is approved by All India Council for Technical Education (AICTE), Accredited by NAAC with 'A' Grde & affiliated to Anna University, Chennai. JPCOE currently offers 7 UG courses in Engineering namely,

1. Computer Science Engineering,
2. Civil Engineering,
3. Electronics and Communication Engineering,
4. Electrical and Electronics Engineering,
5. Mechanical Engineering
6. Information Technology
7. Artificial Intelligence and Data Science

The Institute has well qualified & Experienced staff team creating an ambience for quality education.The entire campus is always very clean and greenery.

ABOUT THE DEPARTMENT

The Department was formally instituted in 2008. The Department has persistently been determined for excellence in teaching and analysis, since the inception of the institute and established itself as one of the reputed departments. The academic activities of the Department encompass practically all major sub-disciplines of Electronics and Communication Engineering.

The Department offers B.E degree in Electronics and Communication Engineering started with an intake of 60 students per year. From 2012 onwards Faculty research interest spans a wide range from abstract theory to down-to-earth problems of immediate interest to industry. Centre of Excellence (CoE) in Embedded and IoT System was established to enhance the skills of the students and faculties. Students here are hence exposed to best learning environment and are provided with in-depth knowledge. It is offering technology oriented courses and creating manpower in the strategic areas well compatible with the industrial expectations.

J.P. COLLEGE OF ENGINEERING

College Road, Ayikudy, Tenkasi – 627 852.
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai
NAAC Accredited with "A" Grade & An ISO 9001: 2015 Certified Institution
Run by DMI Sisters

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROUDLY ORGANIZES

FIVE DAYS ONLINE

FACULTY DEVELOPMENT PROGRAMME (FDP)

ON

"EMERGING TRENDS IN VLSI CHIP DESIGN FOR COMMUNICATION APPLICATIONS USING AI AND ML"

DATE : 20.01.2025 - 24.01.2025

ABOUT THE COURSE

The program "Emerging trends in VLSI chip design for communication applications using AI and ML" likely focuses on the intersection of Very Large Scale Integration (VLSI) chip design with Artificial Intelligence (AI) and Machine Learning (ML) techniques, specifically within communication applications.

OUTCOMES

The outcomes of the program "Emerging Trends in VLSI Chip Design for Communication Applications Using AI and ML" would likely include a combination of technical skills, industry knowledge, and practical expertise. Here are some potential outcomes:

- Understanding VLSI Design Trends: Participants will gain insight into the latest trends and innovations in VLSI chip design tailored for communication systems.
- AI and ML in Hardware: Understanding how AI and ML are revolutionizing hardware design and their role in optimizing chip performance.
- Applications in Communication: Knowledge of how advanced chip designs are used in communication technologies like 5G, IoT, and next-gen wireless systems.
- Problem-Solving with ML: Skills in applying machine learning models to solve challenges in chip design, such as power management, error correction, and real-time processing.
- Alignment with Industry Needs: Awareness of industry requirements and standards in VLSI and communication fields.

TARGET AUDIENCE:

Faculty members , Research scholars , Supervisors, P.G. students and Librarian from Engineering Colleges, All University Departments , Arts & Science Colleges. interested in the Field of AI/ML, Communication and VLSI.

REGISTRATION FEES

Registration is free for all the participants. The number of participants is limited to 100 and the selection is on first-come-first-serve basis.

Registration Link:

https://forms.gle/6DqTNREQraCNJp9A7

IMPORTANT DATES

Last date for the Registration : 18.01.2025
Intimation of selection : 19.01.2025
Conformation by participants : 19.01.2025

SCHEDULE

FACULTY DEVELOPMENT PROGRAM

ON

EMERGING TRENDS IN VLSI CHIP DESIGN FOR COMMUNICATION APPLICATIONS USING AI AND ML

DAY:1 AI/ML ALGORITHM

Dr.T.Prathiba.,
Associate Professor, KCET, Virudhunagar.

DAY:2 VLSI IMPLEMENTATION

Dr.Nelson Kingsley Joel P,
Assistant Professor, JPCOE, Tenkasi.

DAY:3 ADVANCED DIGITAL SYSTEM DESIGN FOR AI APPLICATIONS

Dr.Mathan N,Assistant Professor,Sathyabama Institute of Science &Technology,Chennai

DAY:4 IMPACTS OF MEMS

Dr. Vinoth M, Assistant Professor,
KRCE, Trichirapalli.

DAY:5 VLSI TECHNOLOGY FOR APPLICATION DEVELOPMENT

Dr. B. Viswanathan, Associate Professor,
KRCE, Trichirapalli.

ADDRESS FOR COMMUNICATION

Mrs, M. Shenbagavalli M.Tech., Ph.D.,
Head / ECE,
J.P. College of Engineering ,
Ayikudy , Tenkasi.
Contact No : +91 8668036415